

09/994,004

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,710,264 B2
DATED : March 23, 2004
INVENTOR(S) : Deeney et al.

Page 1 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, showing an illustrative figure, should be deleted and substitute therefor the attached page.

Delete drawing sheet 1-2 and substitute therefor the Drawing Sheets consisting of Fig. 108 as shown on the attached pages.

Signed and Sealed this

Seventeenth Day of May, 2005

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Deeney et al.

(10) Patent No.: **US 6,710,264 B2**
(45) Date of Patent: **Mar. 23, 2004**

(54) **METHOD AND APPARATUS FOR SUPPORTING A CIRCUIT COMPONENT HAVING SOLDER COLUMN INTERCONNECTS USING EXTERNAL SUPPORT**

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(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 83 days.

(21) Appl. No.: **09/994,004**

(22) Filed: **Nov. 16, 2001**

(65) **Prior Publication Data**

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(51) Int. Cl.⁷ **H05K 1/16**

(52) U.S. Cl. **174/260; 361/783**

(58) Field of Search **174/260; 361/783; 257/787-786**

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Thomas J. Augustin et al., patent application filed on Nov. 16, 2001 titled Method And Apparatus For Shock And Vibration Isolation Of A Circuit Component, Attorney Docket No. 10014433-1, pp. 1-15 and 2 sheets of drawings.
Jeffrey L. Deeney et al., patent application filed on Nov. 16, 2001 titled Method And Apparatus Of Supporting Circuit Component Having A Solder Column Array Using Interspersed Rigid Columns, Attorney Docket No. 10015587-1, pp. 1-9 and 1 sheet of a drawing.

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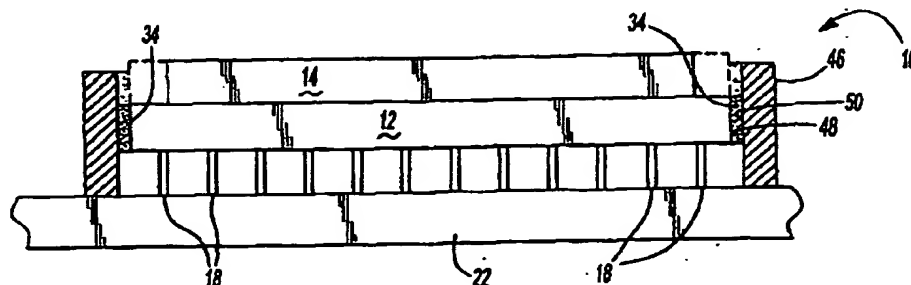
Primary Examiner—Albert W. Paladini

Assistant Examiner—Jeremy Norris

(57) **ABSTRACT**

A circuit board assembly having a circuit board and a column grid array ("CGA") integrated circuit package. The CGA package has a substrate having an array of solder columns extending from a bottom surface. A frame surrounds the CGA integrated circuit package and is affixed thereto. The frame extends from the substrate to a portion of the circuit board when the column grid array integrated circuit package is mounted on the circuit board to support the column grid array integrated circuit package. The frame is affixed to the CGA integrated circuit package by adhesive after the CGA integrated circuit package is mounted on the circuit board, the adhesive accommodating any variations in height of the CGA integrated circuit package.

18 Claims, 2 Drawing Sheets



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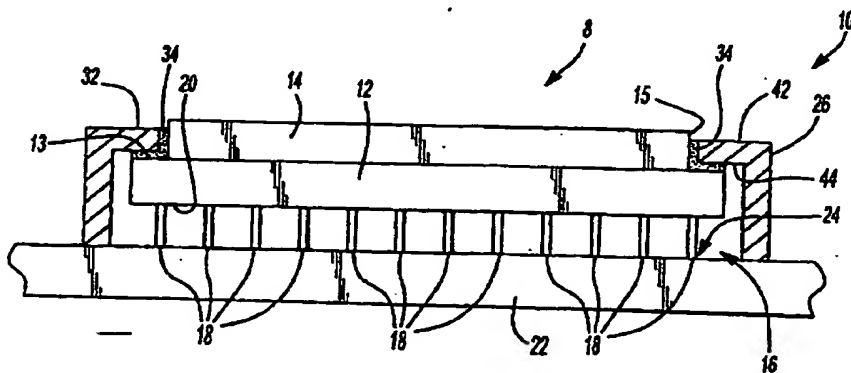


Figure-1

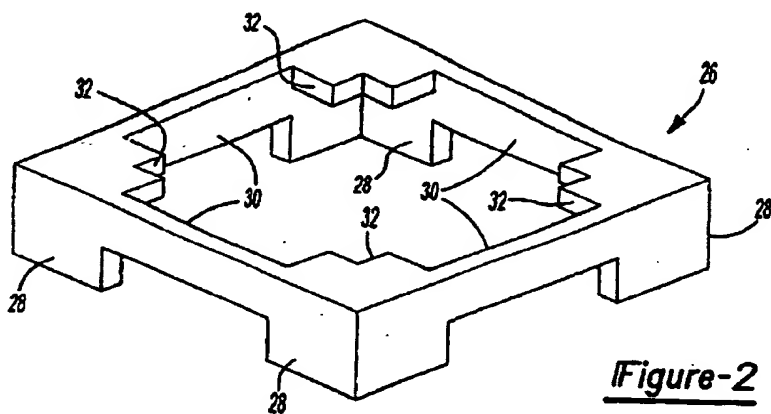


Figure-2

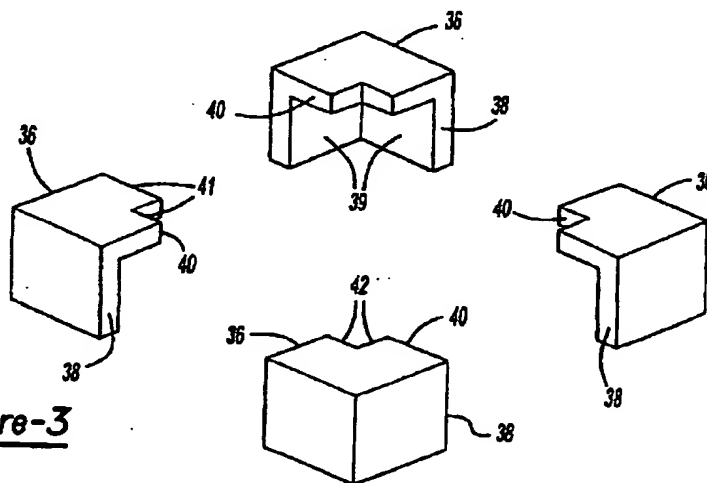


Figure-3

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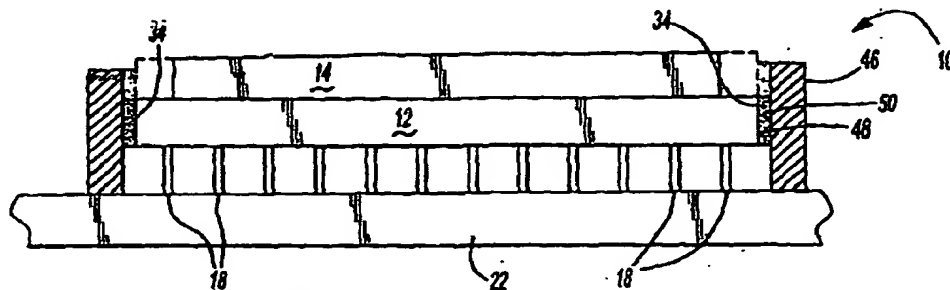


Figure-4

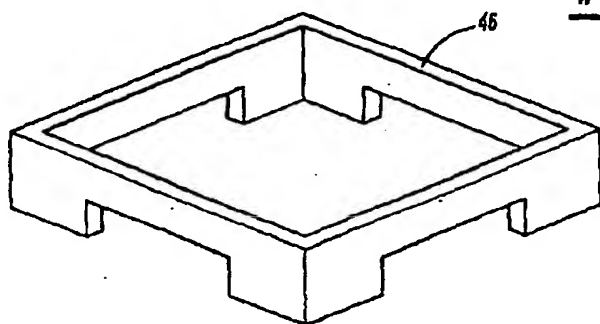


Figure-5

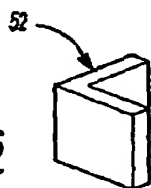


Figure-6

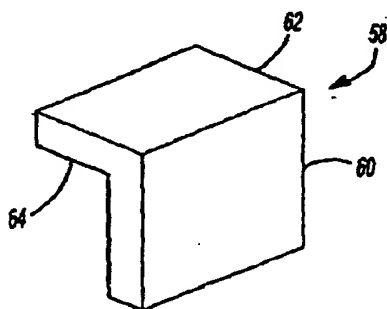
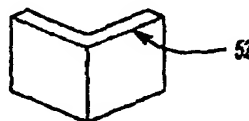
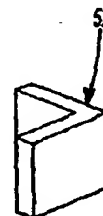
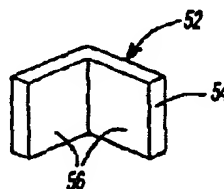


Figure-7

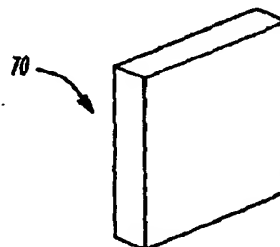


Figure-8